WHAT IS CLAIMED IS:

1. A self-aligned contact structure comprising:

a plurality of spaced apart gate electrodes disposed on a semiconductor substrate with the gate electrodes having opposing first and second sidewalls and top and bottom surfaces, wherein adjacent sidewalls of selected neighboring gate electrodes have respective upper portions that angle toward each other to present a sloped profile;

a first liner layer that is disposed on the semiconductor substrate and covers one of the first and second sidewalls, a minor portion of the other sidewall and a major portion of the top surface of the gate electrodes;

a plurality of self-aligned contact pads that are separately electrically connected to selected regions of the semiconductor substrate, each self-aligned contact pad having opposing upwardly extending sidewalls, wherein a respective self-aligned contact pad is positioned between the selected neighboring gate electrodes , and have a length sufficient so that the self-aligned contact pads extend a distance above the top surface of the gate electrodes;

an interlayer insulation layer disposed on the first liner layer above the top surface and about selected sidewalls of respective gate electrodes, the selected sidewalls of respective gate electrodes being those sidewalls that are positioned away from the self-aligned contact pad electrodes; and

a second liner layer disposed on the angled portions of the adjacent sidewalls of neighboring gate electrodes.

2. The device of claim 1, wherein the gate electrodes are configured so that the second liner layer extends in a generally downward direction in a self-aligned contact window that holds the self aligned contact pad and is configured to extend above the top surfaces of the gate electrodes and down to an impurity diffusion region in the semiconductor substrate.

3. The device of claim 1, wherein the first liner layer has a thickness that is substantially the same over the gate electrodes.

4. The device of claim 1, further comprising a buffer insulation layer positioned proximate an upper portion of respective self-aligned contact pads between the second liner layer and sidewalls of the self aligned contact pad.

5. The device of claim 1, wherein the first and second liner layers comprise silicon nitride and the interlayer insulation layer comprises silicon oxide.

6. The device of claim 4, wherein the first and the second liner layers comprise silicon nitride, and the interlayer insulation layer and the buffer insulation layer comprise silicon oxide.

7. The device of claim 6, wherein the interlayer insulation layer comprises silicon oxide layer and the buffer insulation layer comprises silicon oxide that surrounds an upper portion of the self-aligned contact pad and terminates a distance above the semiconductor substrate.

8. A method of forming the self-aligned contact comprising:

forming gate electrodes that are spaced apart from each other on a semiconductor substrate;

forming a first liner layer on the semiconductor substrate and the gate electrodes;

forming an interlayer insulation layer over the first liner layer;

forming a contact window having opposing spaced apart sidewalls and a bottom by selectively etching the interlayer insulation layer with respect to the first liner layer;

forming a second liner layer over the interlayer insulation layer and the bottom and sidewalls of the contact window;

forming a buffer insulation layer to extend laterally a distance beyond the second liner layer to overhang in the contact window;

exposing the semiconductor substrate between adjacent gate electrodes by performing an etch back process to remove the buffer insulation layer and the second and first insulation layers at a bottom portion of the contact window; and

filling the contact window with conductive material to thereby substantially and/or entirely fill at least a lower portion of the contact window.

9. The method of claim 8, wherein forming the contact window comprises angling the opposing sidewalls thereof so that the sidewalls travel toward each a distance along at least a portion of a length thereof.

10. The method of claim 8, wherein the first and the second liner layers comprise silicon nitride.

11. The method of claim 8, wherein the interlayer insulation layer comprises an oxide layer having a substantially planar surface, and the buffer insulation layer is formed of an oxide layer having an upper surface formed over the interlayer insulation layer disrupted with recesses formed into respective contact windows.

12. The method of claim 8, wherein in the step of forming the contact window by selectively etching the interlayer insulation layer, is carried out so that an upper portion of a gate electrode is etched as well as the first liner layer thereon.

13. The method of claim 8, wherein in the step of exposing the semiconductor substrate is carried out so that the first and second liner layers on the upper and intermediate portions of the sidewalls of the contact window are protected by the buffer insulation layer but the first and second liner layers on the bottom of the contact window are etched away, and wherein, the buffer insulation layer remains on the upper and intermediate portions of the sidewalls of the contact window to form buffer insulation sidewall spacers while the buffer insulation layer on the bottom of the contact window is etched away.

14. The method of claim 8, wherein, after forming the first liner layer and before forming the interlayer insulation layer, the method further comprises:

forming a sacrificial insulation layer;

exposing an upper portion of a gate electrode by etching back the sacrificial insulation layer leaving residual portions of the sacrificial insulation layer;

forming a metal silicide layer on the exposed upper portion of the gate electrode; and

removing the residual portions of the sacrificial insulation layer.

15. A method of forming a self-aligned contact comprising:

forming gate electrodes that are spaced apart from each other with a plurality of the gate electrodes positioned at a cell array region and at least one gate electrode positioned at a peripheral circuit region of the semiconductor substrate, respectively;

forming a first liner layer over the semiconductor substrate and surfaces of the gate electrodes;

forming a sacrificial insulation layer on the first liner layer in an amount sufficient to cover spaces between the gate electrodes of the cell array region;

etching back the sacrificial insulation layer so as to form temporary sidewall spacers on sidewalls of the at least one gate electrode at the peripheral circuit region;

forming a metal silicide layer at least on the semiconductor substrate exposed adjacent the temporary sidewall spacers; then

removing the sacrificial insulation layer remaining at the cell array region and the temporary sidewall spacers of the peripheral circuit region;

forming an interlayer insulation layer having a substantially planar top surface;

selectively etching the interlayer insulation layer with respect to the first liner layer to form at least one contact window in the cell array region between adjacent first and second gate electrodes, the contact window having opposing spaced apart sidewalls and a bottom;

forming a second liner layer on the sidewalls and bottom of the contact window;

forming a buffer insulation layer on the second liner layer so that the buffer insulation layer extends a lateral distance into the contact window to leave a gap space in the contact window, the buffer insulation layer having a greater thickness at a top portion of the sidewalls of the contact window than at a lower portion of the sidewalls of the contact window;

exposing the semiconductor substrate between the gate electrodes of the

cell array region by performing an etch back process; and

filling at least a lower portion of the contact window with conductive material.

16. The method of claim 15, wherein in the step of forming a contact window by selectively etching the interlayer insulation layer, the first liner layer is etched exposing a selected upper portion of the gate electrodes of the cell array region allowing the selected upper portion of the gate electrodes to be removed by the etching while the lower portion is protected from the etching, thereby generating a gate electrode that has an inclined side profile.

17. The method of claim 15, wherein the exposing step is carried out so that the first and/or second liner layers on the upper, intermediate, and/or lower sidewall portions of the contact window are protected by the buffer insulation layer, but the first and second liner layers on the bottom of the contact window are etched away, and wherein the buffer insulation remains on sidewalls of the upper and intermediate portions of the contact window to form sidewall spacers while the buffer insulation layer on the bottom of the contact window is etched away.

18. The method of claim 15, further comprising,

after forming the gate electrodes:

forming lightly doped impurity diffusion regions in the semiconductor substrate at both sides of the gate electrodes using ion implantation; and

after forming the sidewall spacers, performing a second ion implantation process in the peripheral circuit region to form heavily doped impurity diffusion regions, which are spatially positioned proximate the lightly doped impurity diffusion regions, in the semiconductor substrate, at both sides of the temporary sidewall spacers, so that the heavily doped regions reside a greater distance away from the gate electrode than the lightly doped regions.

19. The method of claim 18, wherein the gate electrodes comprise polysilicon, wherein when in an etch back process the sacrificial insulation layer is removed to expose top portions of the gate electrodes at the cell array region and the peripheral circuit region, and the sacrificial insulation layer remains on the

sidewalls of the gate electrodes and on the semiconductor substrate therebetween in the cell array region but is removed with the first liner layer in the peripheral circuit region to expose the semiconductor substrate proximate the sidewall spacers, and wherein a metal silicide layer is concurrently formed on the exposed semiconductor substrate over the heavily doped impurity diffusion regions of the peripheral circuit region and on the exposed top portions of the gate electrodes.

20. The method of claim 15, wherein, after forming the gate electrodes, performing ion implantation to form lightly doped impurity diffusion regions in the semiconductor substrate at both sides of the gate electrodes; and

after forming the temporary sidewall spacers, performing ion implantation to form heavily doped impurity diffusion regions which terminate into the lightly doped impurity diffusion regions of the peripheral circuit region in the semiconductor substrate at both sides of the temporary sidewall spacers.

21. The method of claim 20, wherein the gate electrodes comprise a double-layered structure of polysilicon and tungsten silicide or of polysilicon and tungsten that are sequentially stacked,

wherein in an etch back process after forming the sacrificial insulation layer, the upper portions of the gate electrodes of the cell region and peripheral circuit region are exposed while the sacrificial insulation layer remains on the sidewalls of the gate electrodes and on the semiconductor substrate therebetween, and

wherein the forming the metal silicide layer comprises forming the metal silicide layeron the semiconductor substrate over the heavily doped impurity diffusion regions of the peripheral circuit area.

22. The method of claim 15, after forming the sacrificial insulation layer and before performing the etch back process, the method further comprises forming a photoresist pattern that covers the top surface of the cell array region.

23. The method of claim 15, after forming the metal silicide layer, further comprising a step of forming a protection liner layer thereover for protecting the metal silicide layer.

24. The method of claim 15, further comprising removing at least a portion of the buffer insulation layer from the contact window before filling the contact window with conductive material.

25. The method of claim 23, wherein the first liner layer, the second liner layer, and the protection liner layer comprise silicon nitride.

26. The method of claim 15, wherein the interlayer insulation layer comprises an oxide that is applied to be substantially continuous over the underlying structure with a planar surface, and wherein the buffer insulation layer comprises an oxide that is configured with a substantially planar upper surface and a recess that extends down into the contact window and provides a gap space therein.

27. An integrated circuit assembly, comprising:

a plurality of gate electrodes disposed on a substrate, the gate electrodes having opposing sidewalls and top and bottom surfaces, wherein portions of selected adjacent sidewalls of neighboring electrodes angle generally downwardly and inwardly toward each other while the opposing sidewall of each of the selected sidewalls are substantially linear.

28. An assembly according to claim 27, further comprising;

a plurality of elongate contact windows, a respective one positioned between the selected sidewalls of neighboring electrodes, wherein the contact window sidewalls comprise an angled profile that correspond to the angled gate electrode sidewall configuration; and

a contact pad disposed in each contact window, the contact pad extending generally downwardly and having a length that is greater than the height of the gate electrodes.

29. An assembly according to claim 28, further comprising:

a gate protection liner layer that extends in the contact window and covers the angled sidewall portion of a respective gate electrode; and

a first liner layer that covers the remaining surfaces of the top and opposing sidewalls of the respective gate electrode.

30. An assembly according to claim 29, wherein the angled sidewall is configured on the second sidewall of a first gate electrode and on the first sidewall of the adjacent sidewall of the neighboring second electrode, wherein the first sidewall of the first gate electrode and the second sidewall of the second electrode are generally vertical, wherein the first liner layer covers: (a) greater than a major portion of the top surface of both the first and second gate electrodes; (b) a minor portion of the second sidewall of the first gate electrode and minor portion of the first sidewall of the second gate electrode; and (c) the entire length of the first sidewall of the first electrode and the second sidewall of the second electrode.

31. An assembly according to Claim 29, wherein the bottom surface of the gate electrodes contact the semiconductor substrate, and wherein the remaining external surfaces are covered by at least one of the first and second liner layers so that the gate electrodes are encased.

32. A semiconductor assembly with self-aligned contact pads, comprising:

a cell array region comprising:

first and second gate electrodes disposed on a semiconductor substrate, the first and gate electrodes having opposing first and second sidewalls and top and bottom surfaces, wherein portions of the adjacent sidewalls of the first and second gate electrodes are configured to angle generally downwardly and inwardly toward each other;

a contact window positioned between the adjacent sidewalls of the first and second gate electrodes, wherein the contact window sidewalls comprise an angled profile that correspond to the angled gate electrode sidewalls; and

a contact pad disposed in the contact window, the contact pad extending generally downwardly and having a length that is greater than the height of the gate electrode;

and a peripheral circuit region disposed on the semiconductor substrate

spaced apart from the cell array region, the peripheral circuit region comprising:

at least one gate electrode;

lightly doped impurity diffusion regions in the semiconductor substrate positioned on opposing sides of the at least one gate electrode; and

heavily doped impurity diffusion regions in the semiconductor substrate positioned on opposing sides of the at least one gate electrode so that the heavily doped impurity diffusion regions reside a further distance away from the at least one gate electrode and so that the heavily doped impurity diffusion regions abut the lightly doped impurity diffusion regions.

33. An assembly according to claim 32, further comprising:

a gate protection liner layer that extends along the sidewalls of the contact window and covers the angled sidewall portion of a respective gate electrode in the cell array region; and

a first liner layer that covers target surfaces of the gate electrodes disposed in the cell array region and/or the peripheral circuit region.

34. An assembly according to claim 33, further comprising a buffer insulation layer disposed in an upper and/or intermediate portion of the contact window intermediate the contact pad and the gate protection liner layer.

35. A semiconductor assembly, comprising:

a conductive contact on a substrate in a recess adjacent to a gate electrode having an opposing top and bottom and a gate electrode sidewall that extends from a top surface to the bottom of the sidewall, the gate electrode sidewall angling inwardly from the top surface to an intermediate portion of the sidewall toward the recess with a lower portion of the sidewall being substantially straight so that the bottom of the electrode has a greater width than the top, the conductive contact having a profile that includes the angled shape of the gate electrode sidewall and an upper portion that extends above the top surface of the gate electrode.

36. A method of forming a self-aligned contact window configured to hold a self-aligned contact pad therein in communication with a semiconductor substrate, comprising:

removing a selected portion of an interlayer insulation layer and then an underlying upper portion of adjacent sidewalls of first and second gate electrodes held proximate to each other on a semiconductor substrate to form first and second gate electrodes with sloped sidewalls that angle toward each other and define a portion of the shape of sidewalls of a self-aligned contact window configured to hold a self-aligned contact pad therein.